Dual-Buck Half-Bridge Voltage Balancer

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***Abstract*—Micro-dc grid is a novel power system focused on the development of renewable resources. However, two-wire transmitting power mode is generally accepted in a micro-dc grid, which is usually not suitable for the requirements of the input voltage levels of different power converters and loads. In order to meet the requirements, a half-bridge voltage balancer was introduced in a micro-dc grid, which can convert a two-wire mode into a three-wire mode in a micro-dc grid via a neutral line. However, the shoot-through problem existing in bridge-type converters degrades the reliability of the voltage balancer. In this paper, a dual-buck half-bridge voltage balancer and a control strategy are proposed, which can avoid the shoot-through problem. The small-signal model of the voltage balancer is derived for designing the control parameters and the current relationships of the inductors; the capacitors and the unbalanced loads are analyzed particularly. Finally, a prototype, which can deal with 2-kW unbalance ability, is built to verify that the proposed voltage balancer may have a good ability of balancing the voltage by building a neutral line.**

***Index Terms*—Buck converter, dc distribution system, half bridge, micro-dc grid, voltage balancer.**

I. Introduction

A MICRO-DC grid based on distributed generation system, which can supply superhigh-quality electric power, is widely focused on in recent years with the development of renewable resource generations [1]–[8]. The use of the direct current allows simplifying the insertion between the distribution generation and the network. It needs only one interface converter with alternating current grid to make the operation in islanding mode easier, without compromising the safety of the public network [9], and it has a distinct benefit—a line loss reduction [10]. A micro-dc grid is also dependent on all types of interfacing converter, such as bidirectional converter and dc converter [11], [12], grid-connected inverter [13]–[15], voltage balancer [1]–[7], and so on.

However, a micro-dc grid usually has only one voltage level in two-wire dc distribution system, and it is impossible to supply some types of loads at half voltage such as dc/ac inverters needing a neutral line, converters with input voltage balancing like half-bridge converter and three-level half-bridge converter, and so on. In particular, when a micro-dc grid is used in domestic and office places, a neutral line connected to ground is favorable to the security of the persons. Obviously, in practice, a micro-dc grid with two-wire power system is impossible to meet the requirements of all electronic devices. Thus, a half-bridge voltage balancer was specially introduced to build a neutral line [1]–[7], which can easily convert a two-wire dc grid into a three-wire dc grid by a neutral line. In practice, the voltage balancer may be dispersedly used in any place where the voltage balance is needed, and of course, it can be placed at the output side of the power supply center for building a whole three-wire dc grid. It is thus evident that the voltage balancer improves the quality and flexibility of power supply in a micro-dc grid.

Unfortunately, the topology of bridge-type converters maybe suffers from shoot-through risk, which is a major drawback to the reliability of this type of power converters. A dual-buck half-bridge converter can avoid the shoot-through problem, the freewheeling current goes through the independent freewheeling diodes instead of the body diode of the switches, and all the switches and diodes are operated at half of the line cycle; thus the efficiency may be improved [16]–[21].

In this paper, a dual-buck half-bridge voltage balancer is proposed. For meeting the characteristic of the proposed voltage balancer, a control strategy of respectively driving the two bridge legs of the proposed voltage balancer to work for a high efficiency is also presented. In order to select the parameters of filter inductors and capacitors and to design the control system parameters, the relationships of the currents of inductors, the capacitors, and the unbalanced loads are described in detail, and the small-signal model is derived. Finally, a prototype, which may deal with 2-kW power unbalance ability, is fabricated in the laboratory to verify that the dual-buck half-bridge voltage balancer may have a good ability of balancing the voltage by building a neutral line.

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II. Topology and Control Strategy of the Proposed Voltage Balancer

A. Typical Structure of a Micro-DC Grid

A typical structure of a micro-dc grid [1]–[7] with a voltage balancer is shown in Fig. 1, where the voltage balancer is used to construct a neutral line achieving two same voltage levels for requirements of different types of loads, such as unbalanced loads, half-bridge converter and inverter, and so on.

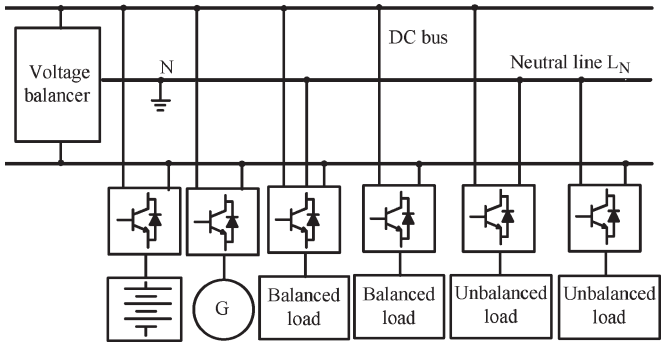

Fig. 1. Typical structure of micro-dc grid.

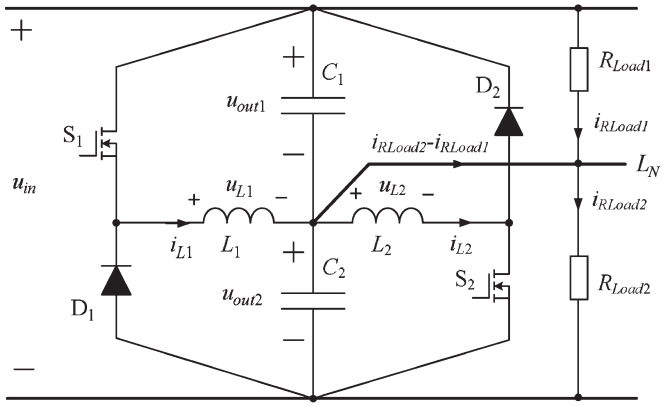

Fig. 2. Proposed dual bulk half-bridge voltage balancer.

B. Proposed Voltage Balancer

The proposed voltage balancer—a dual-buck half-bridge voltage balancer—is shown in Fig. 2, which is made up of a left bridge leg $(\mathrm{S}_1, \mathrm{D}_1, L_1)$, a right bridge leg $(\mathrm{S}_2, \mathrm{D}_2, L_2)$, and a neutral line L_N usually connected to the earth ground. If the complementary driving technology is adopted between the switches S_1 and S_2, the two-inductor currents i_{L1} and i_{L2} will always exist during a switching period, and the unbalanced load current value $(i_{R\mathrm{Load2}} - i_{R\mathrm{Load1}})$ is equal to the different value between the current average value i_{L1} and i_{L2}. Thus, the two-inductor currents will cause additional power losses. Obviously, the complementary operational technology does not use an advantage of the topology to improve the system efficiency. It is very expected to have a control strategy that can drive the left bridge leg and the right bridge leg, respectively, based on the different power quantity of the unbalanced loads.

C. Proposed Control Strategy

The proposed control strategy is presented in Fig. 3. The output signal u_e of the voltage regulator is directly sent to control the switch S_1, and its negative value $(-u_e)$ controls the switch S_2. Combining Figs. 2 and 3, it may be concluded that, when R_{Load2} is lower than R_{Load1}, the signal u_e is positive and the left bridge leg will be driven while the right bridge leg will not work, and on the contrary, the signal u_e is negative and the right bridge leg will be driven. It is thus clear that only one of the two bridge legs will work during every switching period and the loss of the other bridge leg will be avoided compared with the complementary driving technology.

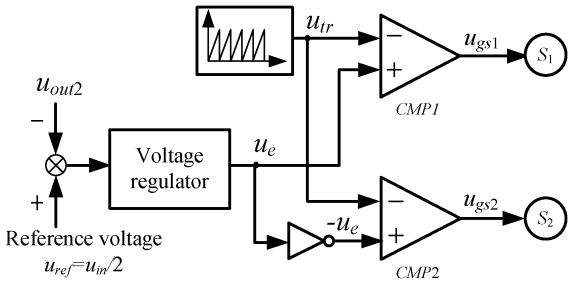

Fig. 3. Diagram of the proposed control strategy.

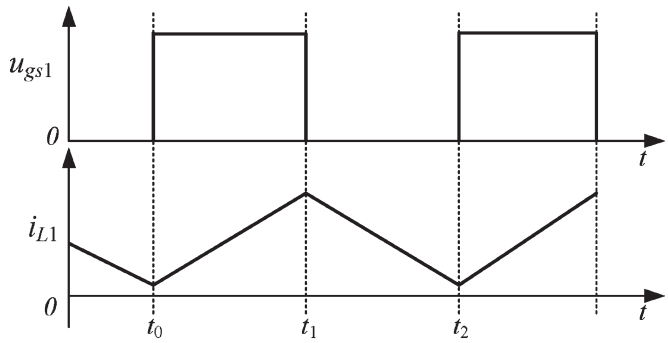

Fig. 4. Driving signal and inductor current waves under CCM.

III. Operating Principle Based on the Proposed Control Strategy

As similar to a buck converter, each bridge leg maybe operates in continuous conduction mode (CCM) and discontinuous mode operation (DCM). For simplifying the analysis of the operational principle, some assumptions are made: 1) All inductors and capacitors are ideal, $C_1 = C_2 = C$, and $L_2 = L_2 = L$; 2) the output voltages u_{out1} and u_{out2} are not changed during each switching process; and 3) all power switches and diodes are the ideal devices with ignored switching time and conduction voltage drop. As the operating procedures of the right bridge leg are the same as those of the left bridge leg, only the analyzing principle of the left bridge leg is given.

A. CCM of Left Bridge Leg

The driving signal u_{gs1}, the current i_{L1}, and the equivalent circuits are shown in Figs. 4 and 5, respectively, during CCM. From Fig. 4, there are only two main operating modes during each switching period.

1) Mode 1 $[t_0, t_1]$ [Refer to Figs. 4 and 5(a)]: The switch S_1 is turned on at the time t_0, and the current i_{L1} increases linearly

$$L_1 \frac{di_{L1}}{dt} = u_{\mathrm{in}} - u_{\mathrm{out2}} = u_{\mathrm{out1}}. \tag{1}$$

During this mode, the input voltage u_{in} sends additional energy to the load R_{Load2} through the inductor L_1. The voltage stress of the freewheeling diode D_1 is the input voltage u_{in}.

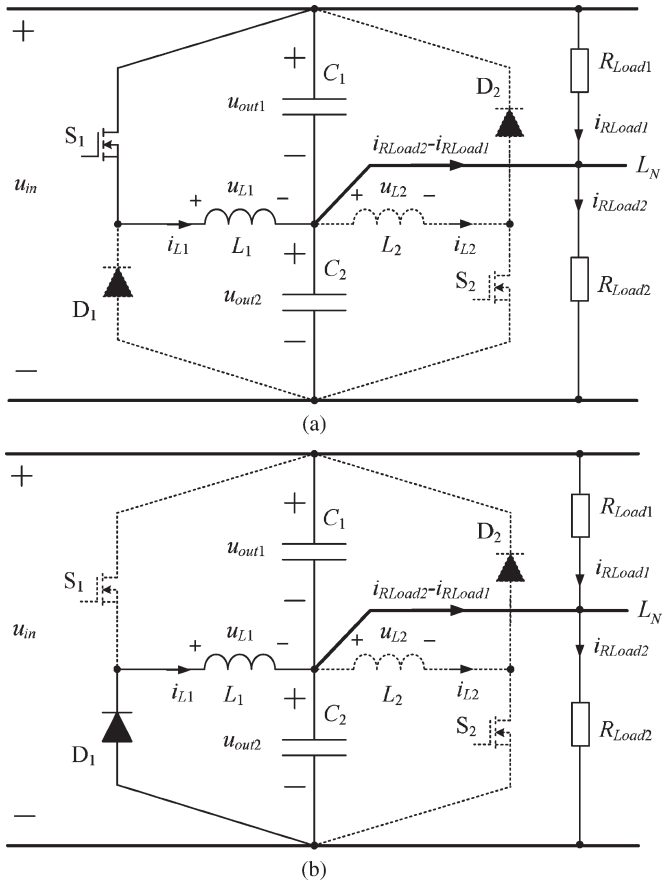

Fig. 5. Equivalent circuits under CCM. (a) Mode 1. (b) Mode 2.

2) Mode 2 $[t_1, t_2]$ [Refer to Figs. 4 and 5(b)]: The switch S_1 is turned off at the time t_1, and the current i_{L1} will continue to run through the freewheeling diode D_1. The current i_{L1} decreases linearly

$$L_1 \frac{di_{L1}}{dt} = -u_{\mathrm{out2}}. \tag{2}$$

The procedure will end when the S_1 is turned on again at the time t_2. During this mode, the voltage stress of the switch S_1 is also the input voltage u_{in}. From the time t_2, a next operating period will start.

As the voltage u_{out1} is the same as u_{out2} under the stabilization and a voltage-second product of an inductor is zero during a period, it can be concluded

$$u_{\mathrm{out1}}(t_1 - t_0) = u_{\mathrm{out2}}(t_2 - t_1). \tag{3}$$

Thus, the time $(t_1 - t_0)$ is equal to the time $(t_2 - t_1)$, i.e., the turn-on time is equal to the turnoff time.

B. DCM of Left Bridge Leg

There are three operating modes under DCM. The u_{gs1}, i_{L1}, and equal circuits are shown in Figs. 5–7, respectively. From Fig. 6, it can be concluded that the mode 1 $[t_0, t_1]$ and the mode 2 $[t_1, t_2]$ are in accordance with the two modes under CCM, respectively. Therefore, only the mode 3 $[t_2, t_3]$ is given.

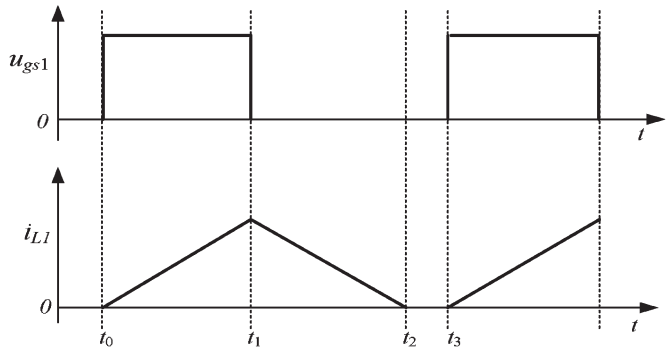

Fig. 6. Driving signal and inductor current waves under DCM.

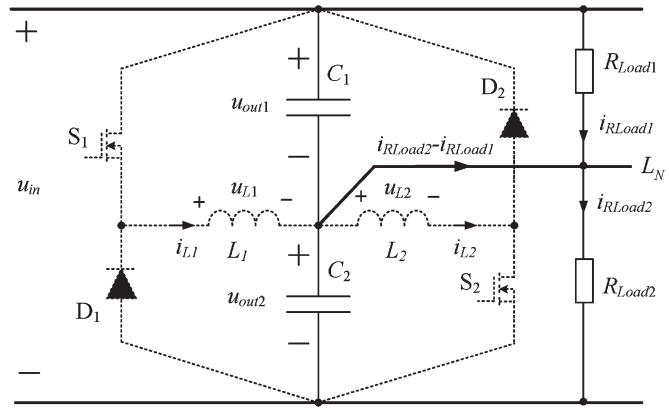

Fig. 7. Equivalent circuit of the mode 3 under DCM.

Mode 3 $[t_2, t_3]$ [Refer to Figs. 6 and 7]: From the time t_2, the loads R_{Load1} and R_{Load2} are supplied by the voltage sources u_{out1} and u_{out2} because the current i_{L1} decreases to zero. According to the voltage-second product of an inductor, it is got from Fig. 6

$$u_{\mathrm{out1}}(t_1 - t_0) = u_{\mathrm{out2}}(t_2 - t_1). \tag{4}$$

Thus, the time $(t_1 - t_0)$ is equal to the time $(t_2 - t_1)$; this means that the turn-on time $(t_1 - t_0)$ is smaller than the turnoff time $(t_3 - t_1)$.

IV. Main Current Relationships

As is known to all, the current relationship of filter inductors and capacitors is the important basis for selecting the value of filter inductors and capacitors and building an average small-signal model in power converters. Therefore, the main current relationships of the voltage balancer will be analyzed in detail. For simplifying the analyses, the current relationships are defined in Fig. 8, and waveforms are shown in Fig. 9. Because of having the similar operating procedure, only the current relationships of the left bridge leg operation is analyzed. The analysis of the current relationships is divided into two parts according to the value of the inductor current i_{L1}.

A. Current i_{L1} Not Zero

The current waveforms are shown in Fig. 9 during the time $(t_0 - t_2)$. As the sum of u_{out1} and u_{out2} is equal to u_{in}, the

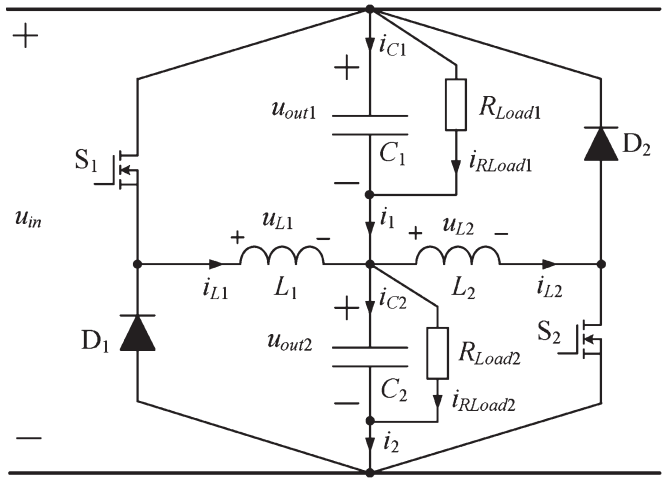

Fig. 8. Assigned diagram of the current relationships.

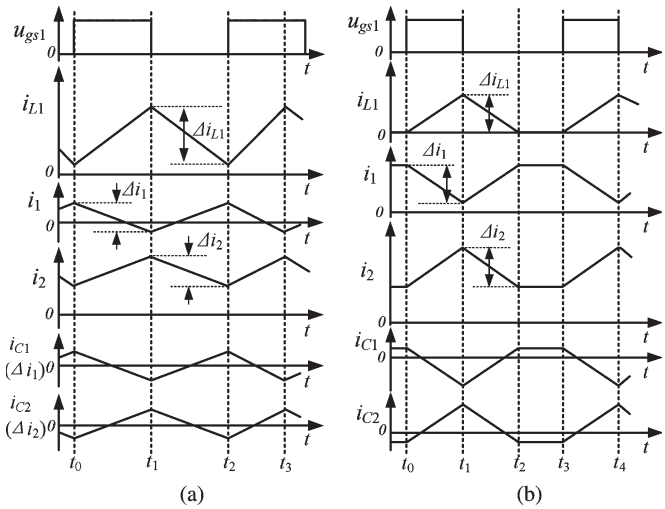

Fig. 9. Main current relationship waveforms of the left bridge leg. (a) CCM. (b) DCM.

ripple voltage $\Delta u_{\rm out1}$ of $u_{\rm out1}$ is also equal to the negative ripple voltage $-\Delta u_{\rm out2}$ of $u_{\rm out2}$

$$\Delta u_{\rm out1} = \frac{1}{C_1}\int_{t_0}^{T_S} i_{C1}\,dt = -\frac{1}{C_2}\int_{t_0}^{T_S} i_{C2}\,dt = -\Delta u_{\rm out2} \quad (5)$$

where $T_S = t_2 - t_0$ in Fig. 9(a) or $T_S = t_3 - t_0$ in Fig. 9(b).

As the average value of the current i_1 is the load current $i_{R\rm Load1}$, the ripple current Δi_1 is equal to the current i_{C1} of the capacitor C_1. Thus, the ripple current Δi_2 is also equal to the current i_{C2} of the capacitor C_2

$$\begin{cases} \Delta i_1 = i_{C1} \\ \Delta i_2 = i_{C2}. \end{cases} \quad (6)$$

According to (5) and (6), it yields under $C_1 = C_2$

$$\Delta i_1 = i_{C1} = -\Delta i_2 = -i_{C2}. \quad (7)$$

As $i_2 = i_1 + i_{L1}$, it can be got

$$\Delta i_{L1} = \Delta i_2 - \Delta i_1 \quad (8)$$

where Δi_{L1} is the ripple current of the inductor L_1. It is obtained by using (7) and (8)

$$\Delta i_{L1} = 2i_{C2} = -2i_{C1}. \quad (9)$$

Therefore, the Δi_{L1} is twice of the currents of i_{C1} and i_{C2}.

B. Current i_{L1} Zero

The current relationships are shown in Fig. 9(b) between the time t_2 and t_3. As i_{L1} is zero, the current i_1 and i_2 will not be associated with the current i_{L1}. That is to say, $i_1 = i_2$.

The powers $P_{\rm out1}$ and $P_{\rm out2}$ of the loads $R_{\rm Load1}$ and $R_{\rm Load2}$ are $u_{\rm out1}^2/R_{\rm Load1}$ and $u_{\rm out2}^2/R_{\rm Load2}$, respectively. As the input power $P_{\rm in}(P_{\rm in} = u_{\rm in} \times i_{\rm in})$ is the sum of $P_{\rm out1}$ and $P_{\rm out2}$ without power losses, the current $i_{\rm in}$ is $(P_{\rm out1} + P_{\rm out2})/u_{\rm in}$, which is equal to i_1 and i_2. Due to $u_{\rm out1} = u_{\rm out2}$ and $R_{\rm Load2} < R_{\rm Load1}$ under stable condition, we can get $i_2 < i_{R\rm Load2}$ and $i_1 > i_{R\rm Load1}$. Thus, the capacitor C_2 supplies a current $(i_{C2} = i_{R\rm Load2} - i_2)$ to the load $R_{\rm Load2}$ by discharging, which results in the $u_{\rm out2}$ linearly falling down, whereas the capacitor C_1 is charged by the current $(i_{C1} = i_1 - i_{R\rm Load1})$, and the $u_{\rm out1}$ linearly rises. Because of $u_{\rm out1} + u_{\rm out2} = u_{\rm in}$, the $\Delta u_{\rm out1}$ and i_{C1} are also equal to $-\Delta u_{\rm out2}$ and $-i_{C2}$, respectively.

V. Average Small-Signal Model

In order to select the control system parameters, the average small-signal model of the voltage balancer under CCM is derived. The duty cycles of S_1 and S_2 are defined as $d_1(d_1 = D_1 + \hat{d}_1)$ and $d_2(d_2 = D_2 + \hat{d}_2)$, respectively, where D_1, D_2, $\hat{d}_1$, and $\hat{d}_2$ are stable duty ratios and the perturbations of d_1 and d_2. Moreover, the voltage $u_{\rm in}$ and $u_{\rm out2}$ are defined as $u_{\rm in} = U_{\rm in} + \hat{u_{\rm in}}$ and $u_{\rm out2} = U_{\rm out2} + \hat{u_{\rm out2}}$, respectively, where $U_{\rm in}$, $U_{\rm out2}$, $\hat{u_{\rm in}}$, and $\hat{u_{\rm out2}}$ are the stable voltage values and the perturbations of $u_{\rm in}$ and $u_{\rm out2}$.

A. Average Small-Signal Model of Left Bridge Leg

From Fig. 8, we can obtain (10) and (11) when the left bridge leg operates under CCM.

1) S_1 turning on

$$\begin{cases} u_{L1} = L_1\frac{di_{L1}}{dt} = u_{\rm in} - u_{\rm out2} \\ i_{C2} = C_2\frac{du_{\rm out2}}{dt} = i_{L1} + C_1\frac{d(u_{\rm in}-u_{\rm out2})}{dt} + \frac{u_{\rm in}-u_{\rm out2}}{R_{\rm load1}} - \frac{u_{\rm out2}}{R_{\rm Load2}}. \end{cases} \quad (10)$$

2) S_1 turning off

$$\begin{cases} u_{L1} = L_1\frac{di_{L1}}{dt} = u_{\rm in} - u_{\rm out2} \\ i_{C2} = C_2\frac{du_{\rm out22}}{dt} = i_{L1} + C_1\frac{d(u_{\rm in}-u_{\rm out2})}{dt} + \frac{u_{\rm in}-u_{\rm out2}}{R_{\rm load1}} - \frac{u_{\rm out2}}{R_{\rm Load2}}. \end{cases} \quad (11)$$

According to the methods of building average model, it can be derived from (10) and (11)

$$\begin{cases} L\frac{d\hat{i}_{L1}}{dt} = D_1\hat{u}_{\rm in} + \hat{d}_1 U_{\rm in} - \hat{u}_{\rm out2} \\ 2C\frac{d\hat{u}_{\rm out2}}{dt} = \hat{i}_{L1} + C\frac{d\hat{u}_{\rm in}}{dt} + \frac{\hat{u}_{\rm in}}{R_{\rm Load1}} - \left(\frac{1}{R_{\rm Load1}} + \frac{1}{R_{\rm Load2}}\right)\hat{u}_{\rm out2}. \end{cases} \quad (12)$$

Thus, the transfer function of the output voltage $u_{\text{out}2}$ versus the duty cycle d_1 is presented by

$$G_{\text{out}2d1}(s) = \left.\frac{\hat{u}_{\text{out}2}(s)}{\hat{d}_1(s)}\right|_{\hat{u}_{\text{in}}(s)=0} = \frac{U_{\text{in}}}{2LCS^2 + LS\left(\frac{1}{R_{\text{Load}1}} + \frac{1}{R_{\text{Load}2}}\right) + 1}. \quad (13)$$

It is obvious that the transfer function is similar to that of a buck converter.

B. Average Small-Signal Model of Right Bridge Leg

From Fig. 8, (14) and (15) may be got when the right bridge leg operates under CCM.

1) S_2 turning on

$$\begin{cases} u_{L2} = L_2 \frac{di_{L2}}{dt} = u_{\text{out}2} \\ i_{C2} = C_2 \frac{du_{\text{out}2}}{dt} = C_1 \frac{d(u_{\text{in}} - u_{\text{out}2})}{dt} + \frac{u_{\text{in}} - u_{\text{out}2}}{R_{\text{load}1}} - \frac{u_{\text{out}2}}{R_{\text{Load}2}} - i_{L2}. \end{cases} \quad (14)$$

2) S_2 turning off

$$\begin{cases} u_{L2} = L_2 \frac{di_{L2}}{dt} = (u_{\text{in}} - u_{\text{out}2}) \\ i_{C2} = C_2 \frac{du_{\text{out}2}}{dt} = C_1 \frac{d(u_{\text{in}} - u_{\text{out}2})}{dt} + \frac{u_{\text{in}} - u_{\text{out}2}}{R_{\text{load}1}} - \frac{u_{\text{out}2}}{R_{\text{Load}2}} - i_{L2}. \end{cases} \quad (15)$$

According to the methods of building average model, (14) and (15) are rewritten by

$$\begin{cases} L\frac{d\hat{i}_{L2}}{dt} = \hat{u}_{\text{out}2} - (1 - D_2)\hat{u}_{\text{in}} + \hat{d}_2 U_{\text{in}} \\ 2C\frac{d\hat{u}_{\text{out}2}}{dt} = C\frac{d\hat{u}_{\text{in}}}{dt} + \frac{\hat{u}_{\text{in}}}{R_{\text{Load}1}} - \left(\frac{1}{R_{\text{Load}1}} + \frac{1}{R_{\text{Load}2}}\right)\hat{u}_{\text{out}2} - \hat{i}_{L2}. \end{cases} \quad (16)$$

The transfer function of the output voltage $u_{\text{out}2}$ versus the duty cycle d_2 is given by

$$G_{\text{out}2d2}(s) = \left.\frac{\hat{u}_{\text{out}2}(s)}{\hat{d}_2(s)}\right|_{\hat{u}_{\text{in}}(s)=0} = \frac{-U_{\text{in}}}{2LCS^2 + LS\left(\frac{1}{R_{\text{Load}1}} + \frac{1}{R_{\text{Load}2}}\right) + 1}. \quad (17)$$

Comparing (13) and (17), the right bridge leg is running backward buck converter. Moreover, combining Fig. 3, (13), and (17), the control system diagram of the voltage balancer can be illustrated by Fig. 10, where K_m is the amplitude of the unipolar triangle carrying wave u_{tr}, k is the feedback coefficient, and

$$G_{\text{out}2d}(S) = \frac{U_{\text{in}}}{2LCS^2 + LS\left(\frac{1}{R_{\text{Load}1}} + \frac{1}{R_{\text{Load}2}}\right)}.$$

It is obvious that $G_{\text{out}2d}(S)$ is similar to the transfer function of a buck converter, and thus, the designing method of the control system parameters of the voltage balancer may be according to that of a buck converter.

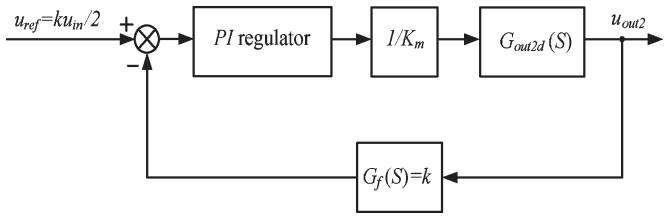

Fig. 10. Control system diagram.

VI. Simulation Results

In order to confirm the aforementioned analysis, the computer simulations of the main current relationships and the loads transiently changing are carried out by using software Saber, and the other condition simulations are ignored. Considering single phase 110 V for a half-bridge inverter and single phase 220 V for a full-bridge inverter, the dc bus voltage (input voltage u_{in}) is selected to be 360 V. The other main simulation parameters are listed: switching frequency of 25 kHz, $L_1 = L_2 = 230\ \mu$H, and $C_1 = C_2 = 470\ \mu$F.

A. Simulations of the Current Relationships

In this section, only the simulation results of the current relationships of the left bridge leg are given. The simulation results of the current relationships are given in Fig. 11.

In Fig. 11, it includes CCM [$R_{\text{Load}1} = 100\ \Omega$ and $R_{\text{Load}2} = 10\ \Omega$ as shown in Fig. 10(a)] and DCM [$R_{\text{Load}1} = 40\ \Omega$ and $R_{\text{Load}2} = 30\ \Omega$ as shown in Fig. 11(b)]. As seen from Fig. 11, under nonzero i_{L1}, it can be easily concluded that $\Delta u_{\text{out}1} = -\Delta u_{\text{out}2}$, $i_{C1} = i_{C2}$, and $\Delta i_{L1} = i_{C2} - i_{C1}$.

When the inductor current i_{L1} is zero, we can get $P_{\text{out}1} = u_{\text{out}1}^2/R_{\text{Load}1} = 810$ W, $P_{\text{out}2} = u_{\text{out}2}^2/R_{\text{Load}2} = 1080$ W, $i_{\text{in}} = (P_{\text{out}1} + P_{\text{out}2})/u_{\text{in}} = 5.25$ A, $i_2 = i_1 = i_{\text{in}} = 5.25$ A, $i_{R\text{Load}1} = u_{\text{out}1}/R_{\text{Load}1} = 4.5$ A, and $i_{R\text{Load}2} = u_{\text{out}2}/R_{\text{Load}2} = 6$ A under steady state. Because of $i_2 < i_{R\text{Load}2}$, the lacking current ($i_2 - i_{R\text{Load}2} = -0.75\ \text{A} = i_{C2}$) is supplied by the capacitor C_2 discharging, and the voltage $u_{\text{out}2}$ linearly drops. Due to $i_1 > i_{R\text{Load}1}$, the capacitor C_1 is charged by the surplus current ($i_1 - i_{R\text{Load}1} = 0.75\ \text{A} = i_{C1}$), and the voltage $u_{\text{out}1}$ linearly rises. These states are presented in Fig. 11(b).

B. Simulations of Loads Instantly Changing

Fig. 12 shows the simulation results of loads transiently changing, where Fig. 12(a) gives the results of the load current $i_{R\text{Load}2} = 2.3$ A and the load current $i_{R\text{Load}1}$ changes from 0 to 6.7 A; Fig. 12(b) describes the results of $i_{R\text{Load}1} = 1.8$ A, and the $i_{R\text{Load}2}$ changes from 0 to 5 A.

As seen from Fig. 12, the left bridge leg will operate when $i_{R\text{Load}2}$ is larger than $i_{R\text{Load}1}$; otherwise, the right bridge leg will run. At the same time, the output voltages $u_{\text{out}1}$ and $u_{\text{out}2}$ are nearly equal, although they have obvious fluctuations when the loads are instantly changed. The fluctuations are mainly

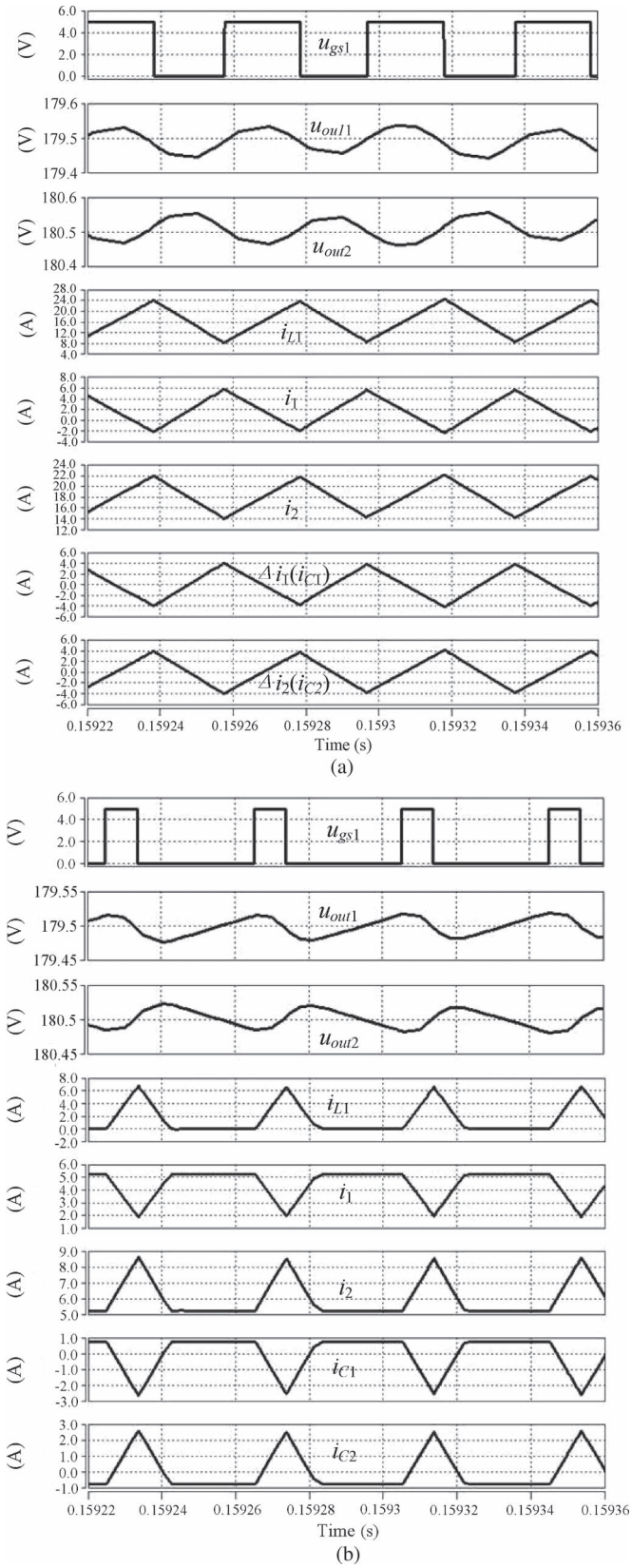

Fig. 11. Simulation results of the current relationships under the left bridge leg operation. (a) CCM. (b) DCM.

caused by a longer regulated time of the voltage regulator whose output signal polarity is altered under transiently changing loads as seen from Fig. 3.

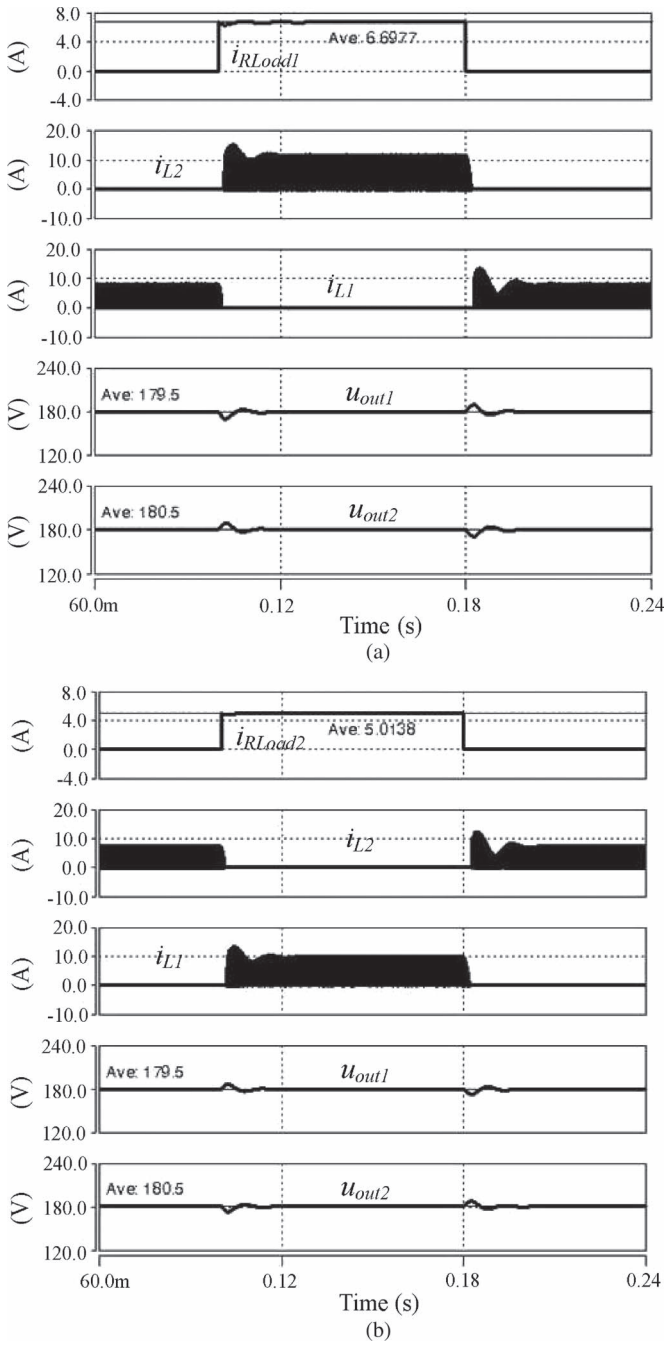

Fig. 12. Simulation results under loads transiently changing. (a) R_{Load1} transiently changing. (b) R_{Load2} transiently changing.

VII. Experimental Results

A dual-buck half-bridge voltage balancer has been built to verify the results of the analysis. The switches S_1 and S_2 and the freewheeling diodes D_1 and D_2 are selected to be SPW47N60C3 and DSEI60-06A, respectively. The other main parameters are the same as the parameters used in the simulation.

Fig. 13 shows the experimental results under the left bridge leg operation (CCM: $i_{R\mathrm{Load1}} = 1.8$ A, $i_{R\mathrm{Load2}} = 12.0$ A, $u_{\mathrm{out1}} = 180.1$ V, and $u_{\mathrm{out2}} = 180.1$ V; DCM: $i_{R\mathrm{Load1}} = 2.8$ A, $i_{R\mathrm{Load2}} = 6.0$ A, $u_{\mathrm{out1}} = 180.5$ V, and $u_{\mathrm{out2}} = 180.3$ V).

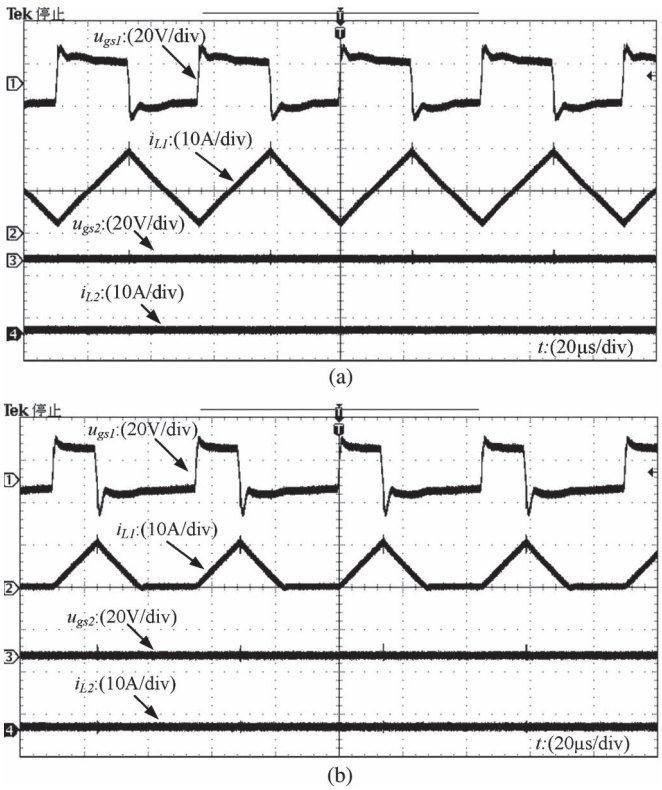

Fig. 13. Experimental results under the left bridge leg operation. (a) CCM. (b) DCM.

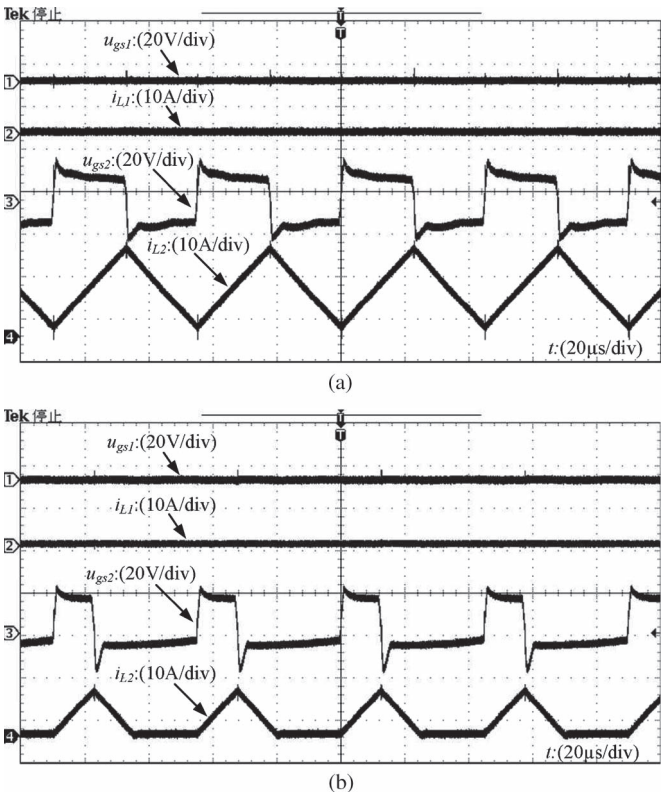

Fig. 14. Experimental results under the right bridge leg operation. (a) CCM. (b) DCM.

Fig. 14 gives the experimental results under the right bridge leg operation (CCM: $i_{R\mathrm{Load1}} = 12.7$ A, $i_{R\mathrm{Load2}} = 2.4$ A, $u_{\mathrm{out1}} = 179.6$ V, and $u_{\mathrm{out2}} = 179.7$ V; DCM: $i_{R\mathrm{Load1}} =$

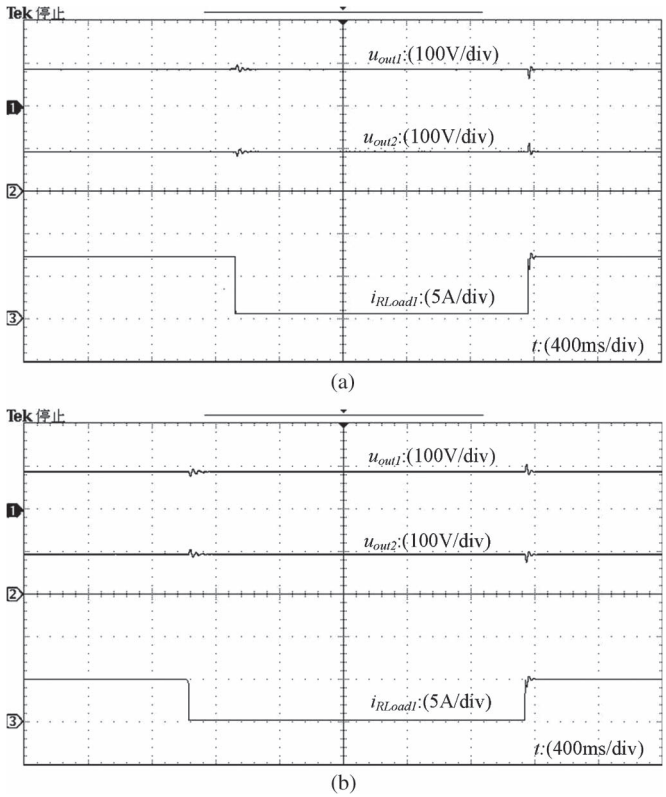

Fig. 15. Experimental results under transiently changing loads. (a) Changing $R_{\mathrm{Load1}}(i_{R\mathrm{Load2}} = 2.3$ A). (b) Changing $R_{\mathrm{Load2}}(i_{R\mathrm{Load1}} = 1.8$ A).

TABLE I
EXPERIMENTAL DATA UNDER LEFT BRIDGE LEG OPERATION

u_{out1} (V)	i_{RLoad1} (A)	u_{out2} (V)	i_{RLoad2} (A)	Δu (V)
179.7	0.72	180.0	1.98	-0.3
176.2	0.71	176.7	3.62	-0.5
180.5	2.80	180.3	6.0	0.2
180.1	1.80	180.0	12.0	0.1

4.5 A, $i_{R\mathrm{Load2}} = 2.0$ A, $u_{\mathrm{out1}} = 180.0$ V, and $u_{\mathrm{out2}} = 179.8$ V). From Figs. 13 and 14, it can be obtained that the experimental results are in accordance with the analysis under CCM and DCM.

Fig. 15 shows the experimental waveforms when the loads R_{Load1} and R_{Load2} are transiently changed, respectively, where u_{out1} and u_{out2} are 179.7 and 179.8 V before changing R_{Load1} and are 179.6 and 179.8 V after changing R_{Load1} in Fig. 15(a); u_{out1} and u_{out2} are 179.6 and 179.8 V before changing R_{Load2} and are 179.7 and 180.1 V after changing R_{Load2} in Fig. 15(b). Fig. 15 indicates that the proposed voltage balancer using the proposed control strategy can well maintain the voltage balance when the loads are transiently changed. Moreover, we can see that the output voltages have a distinct ripple, which is caused by a long dynamic response time as seen from Fig. 3.

Tables I and II list the experimental data under the different input voltages and loads, where $\Delta u = u_{\mathrm{out1}} - u_{\mathrm{out2}}$. These experimental data indicate that the proposed voltage balancer can achieve a good balancing ability.

TABLE II
EXPERIMENTAL DATA UNDER RIGHT BRIDGE LEG OPERATION

u_{out1} (V)	i_{RLoad1} (A)	u_{out2} (V)	i_{RLoad2} (A)	Δu (V)
181.6	1.52	181.4	0.87	0.2
177.1	3.20	177.4	0.84	-0.3
179.6	6.70	179.8	2.30	-0.2
179.6	12.70	179.7	2.40	-0.1

VIII. CONCLUSION

In this paper, a dual-buck half-bridge voltage balancer and its control strategy are proposed. This type of voltage balancer can well resolve the shoot-through problem. It can build a neutral line to balance two output voltages for different loads in a micro-dc grid. At last, the simulation and experimental results are done to illustrate the proposed voltage balancer having a good ability of balancing output voltage even if under the different input voltage, unbalanced loads, and transiently changing loads.

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